IP and FPGA Verification

Blue Pearl Software

Analyze-RTL Linting™ Solution

Overview

The Blue Pearl Software Suite is a set of analysis and debugging tools for IP and FPGA verification that finds:

- RTL design errors and problems
- Missing Clock Domain Crossing (CDC) synchronization
- False and multi-cycle path timing exceptions

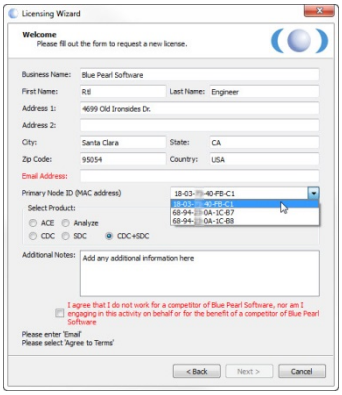
Why Analyze-RTL Linting solution

FPGAs routinely have millions of gates with memories, transceivers, third party IP and processor cores. Problems can be time consuming and complex to debug in the lab and through simulations. To reduce verification and debug times, designers need tools that can identify problems quickly before simulation and synthesis, and definitely before spending time in the lab.

Features of Analyze-RTL Linting solution

With Analyze-RTL Linting solution, designers can

- Get effective and meaningful results quickly with tool Setup Wizard

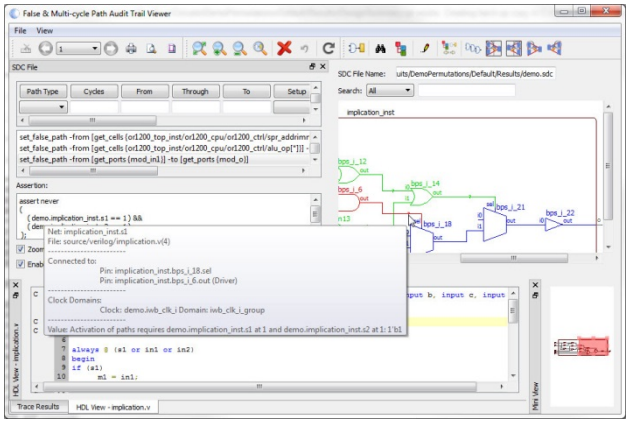


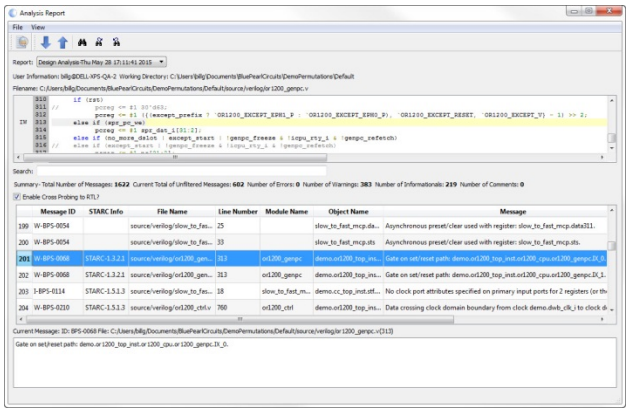
- Check IEEE Verilog/System Verilog & VHDL language specification compliance and syntax
- Configure checks along with standard checks, STARC, RMM, and Xilinx UltraFast
- Use the GUI to streamline debug; integrated RTL, schematics, and message viewer
- Use easy debug message sorting, filtering and waiving to pinpoint problems
- Automate flow with Command Line Interface (CLI), and re-usable message waiver file

Debug Design Issues Quickly

The Visual Verification Environment enables Analyze RTL solution users to debug design issues quickly using intelligent sorting and message filtering.

- Low noise
- Check customization for specific design style
- Easy setup
- Waiver migration

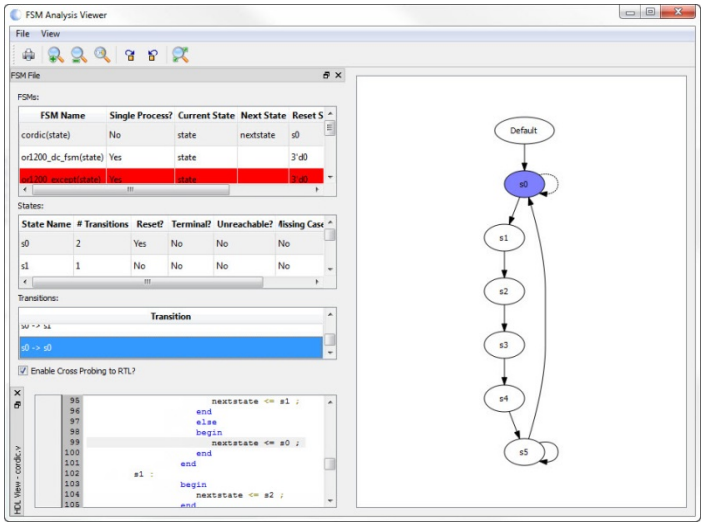




Finite State Machine Analysis

Rather than writing exhaustive simulation test benches to validate their finite state machines (FSMs), designers can use the FSM analysis capability within Analyze-RTL Linting solution. With minimal effort, designers can

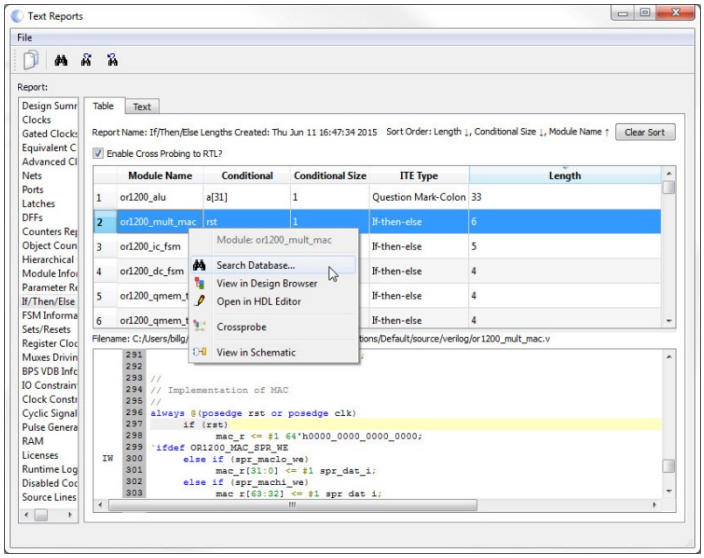
- Extract FSMs from their RTL
- Find dead or unreachable states
- Generate easy to read bubble diagrams to better visualize FSMs



RTL Checks for High Speed Designs

It is important to find as early as possible RTL coding that prevents the design from getting desired speed. FPGAs, because of their more constrained fabric than ASIC, certain type of structures causes slow down. Rather than wait for synthesis or static timing analysis results, Analyze-RTL Linting solution users can easily identify:

- High fanout nets
- Deep nested “if-then-else” statements
- High levels of logic paths
- Reset methodology, Async/sync



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